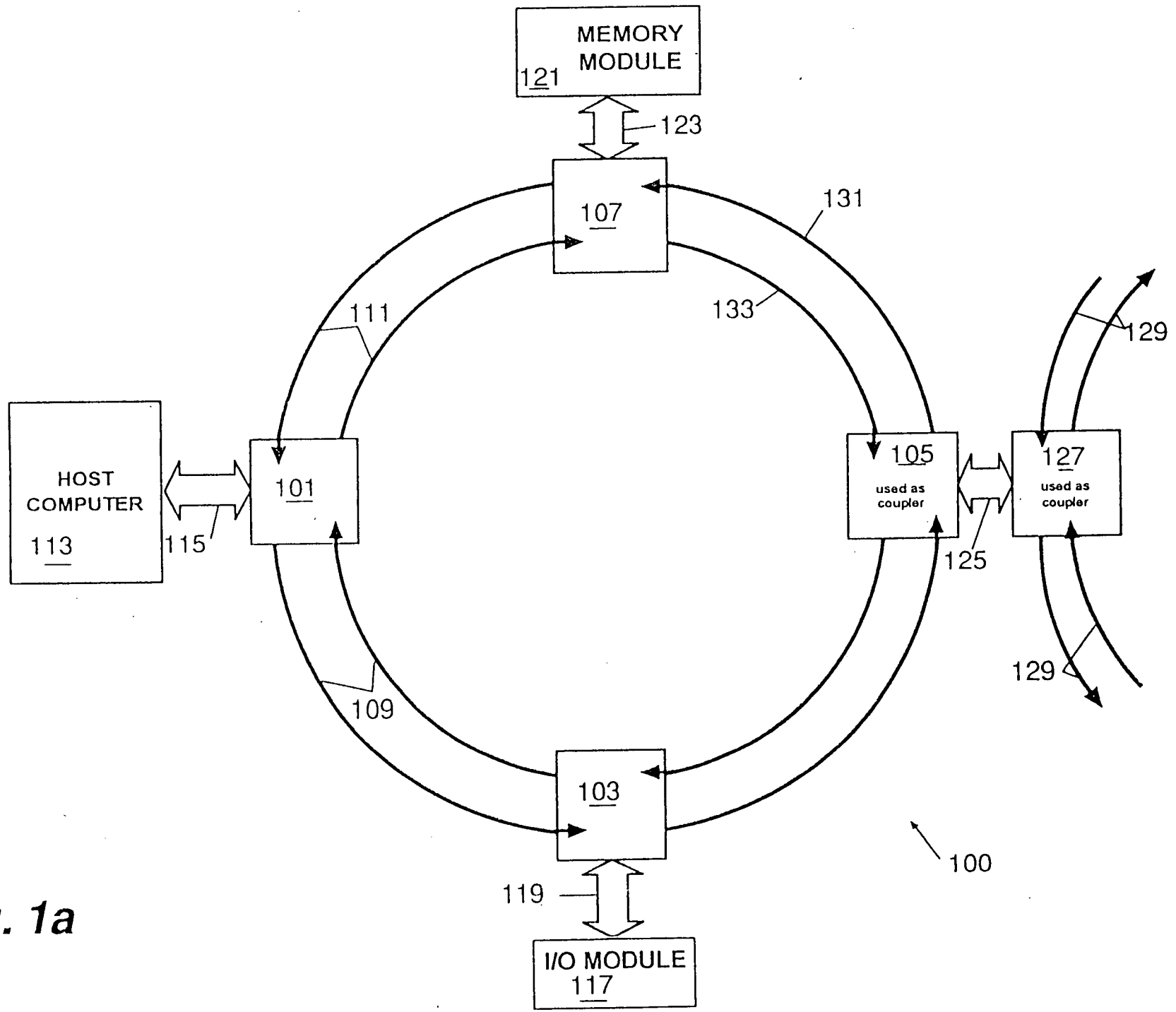

MEMORY MODULE
121
123
107
131
111
133
129
HOST COMPUTER
113
115
101
105
used as coupler
127
used as coupler
125
129
109
103
100
119
I/O MODULE
117

Fig. 1a

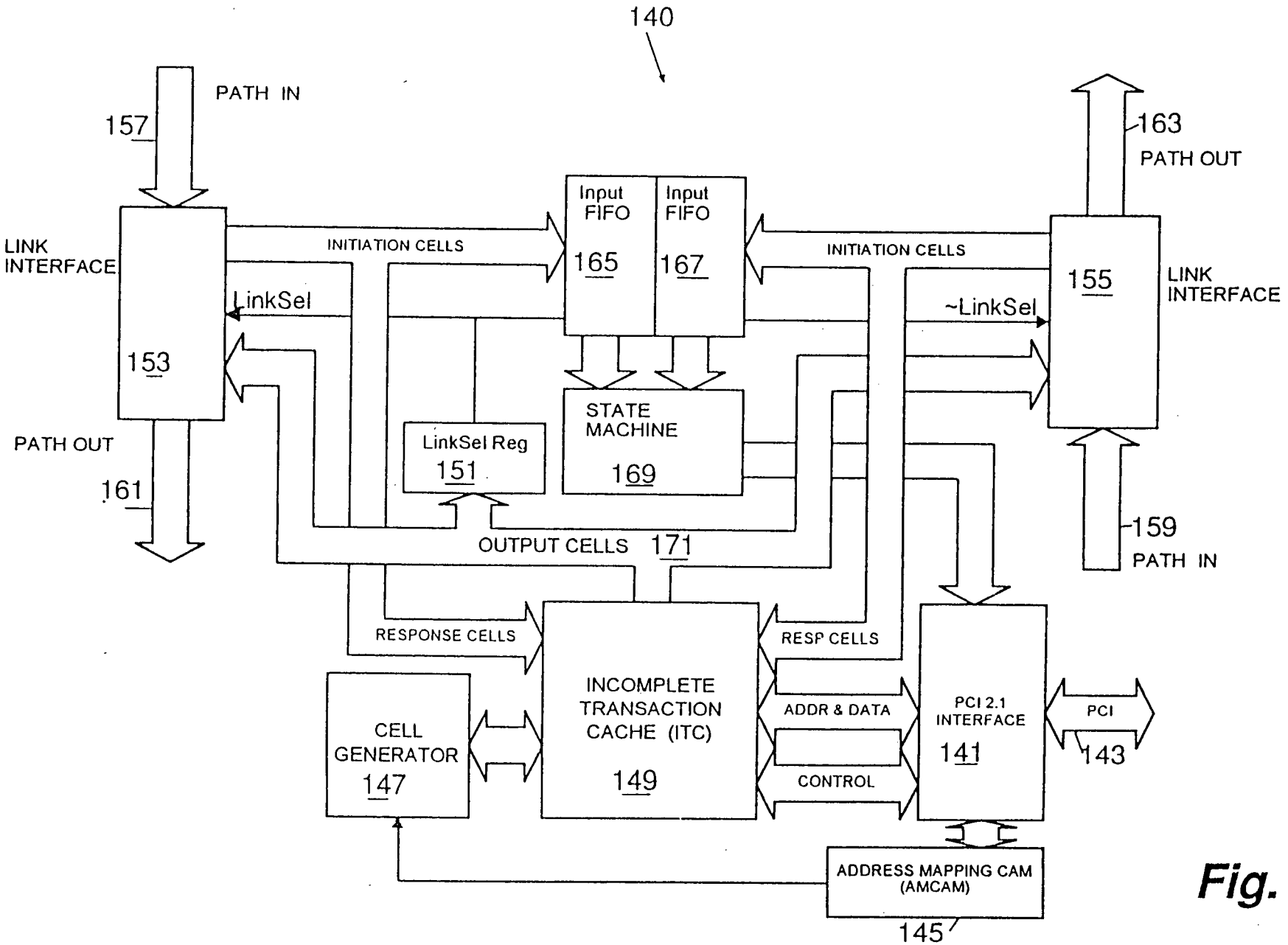


Fig. 1b

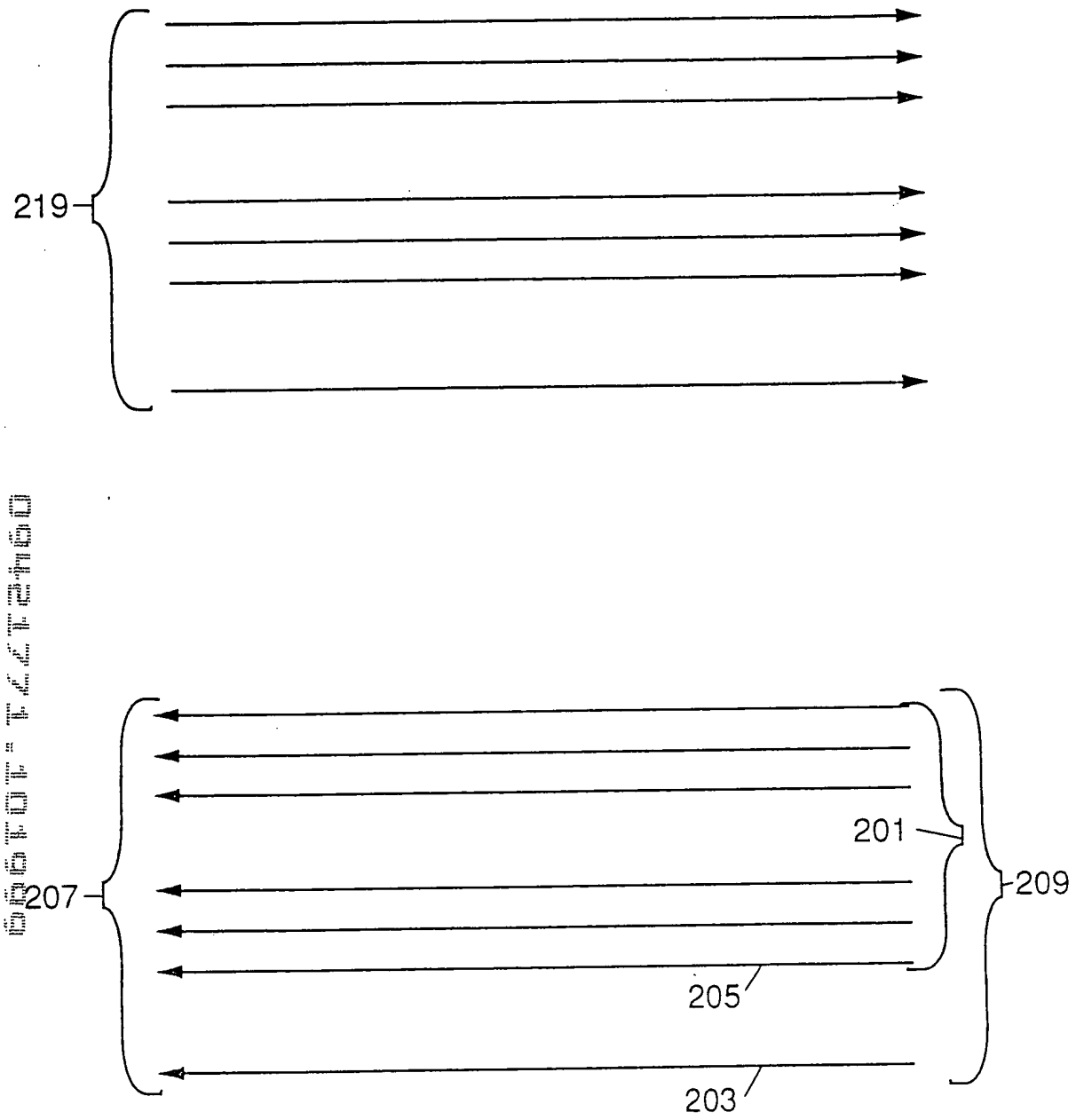


Fig. 2

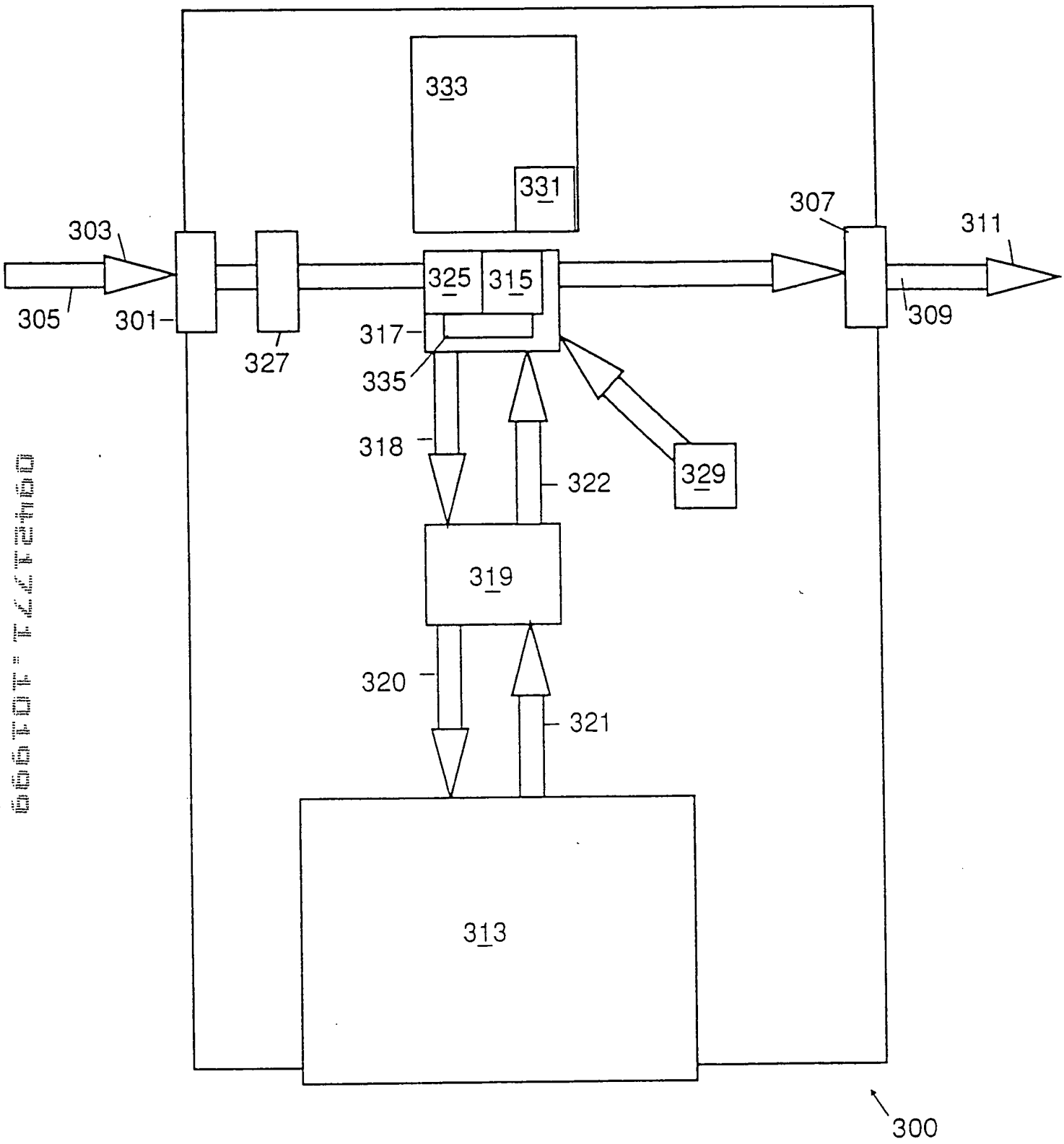

333
331
303
307
311
305
301
325
315
309
327
317
335
318
322
329
319
320
321
313
300

Fig. 3

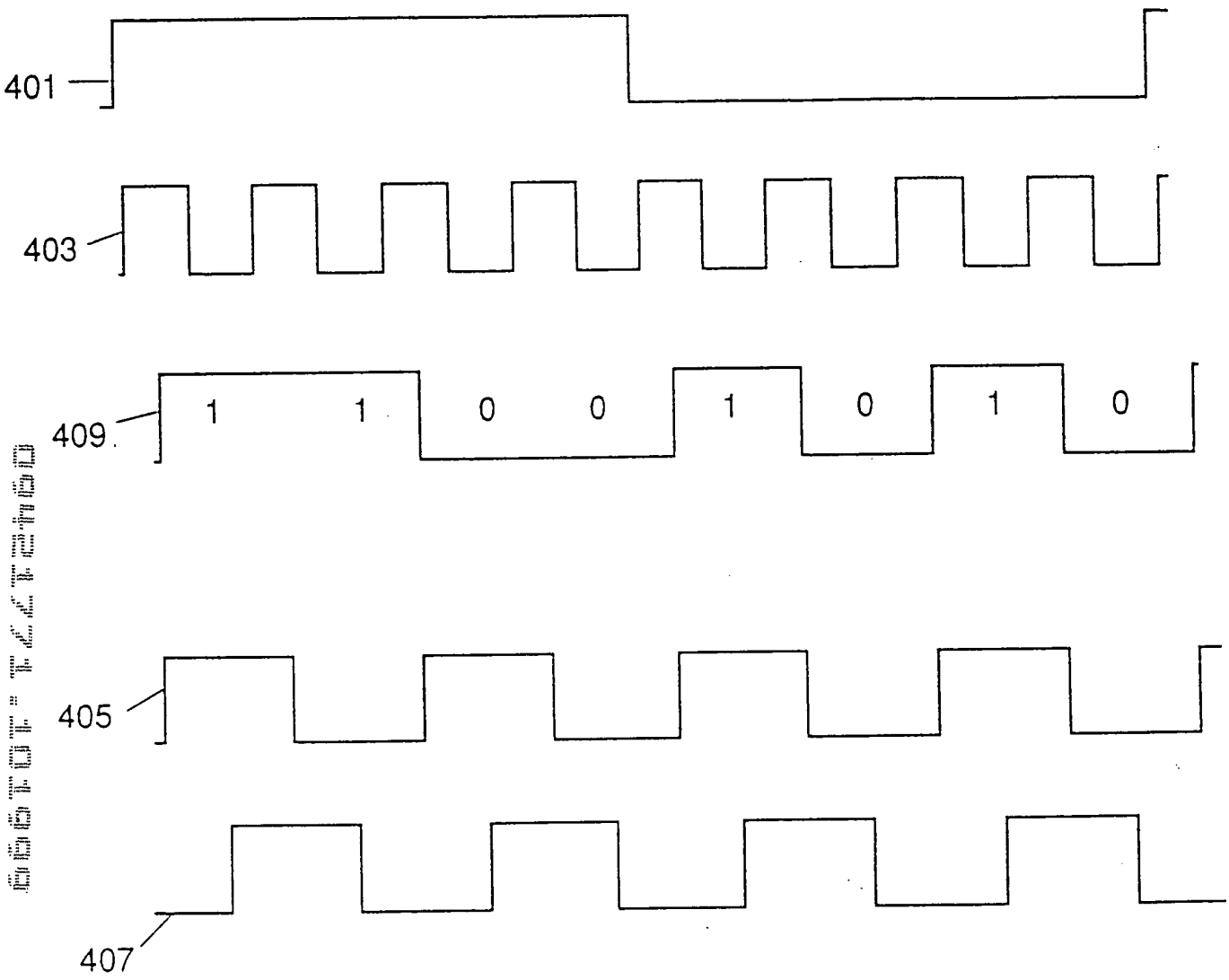


Fig. 4

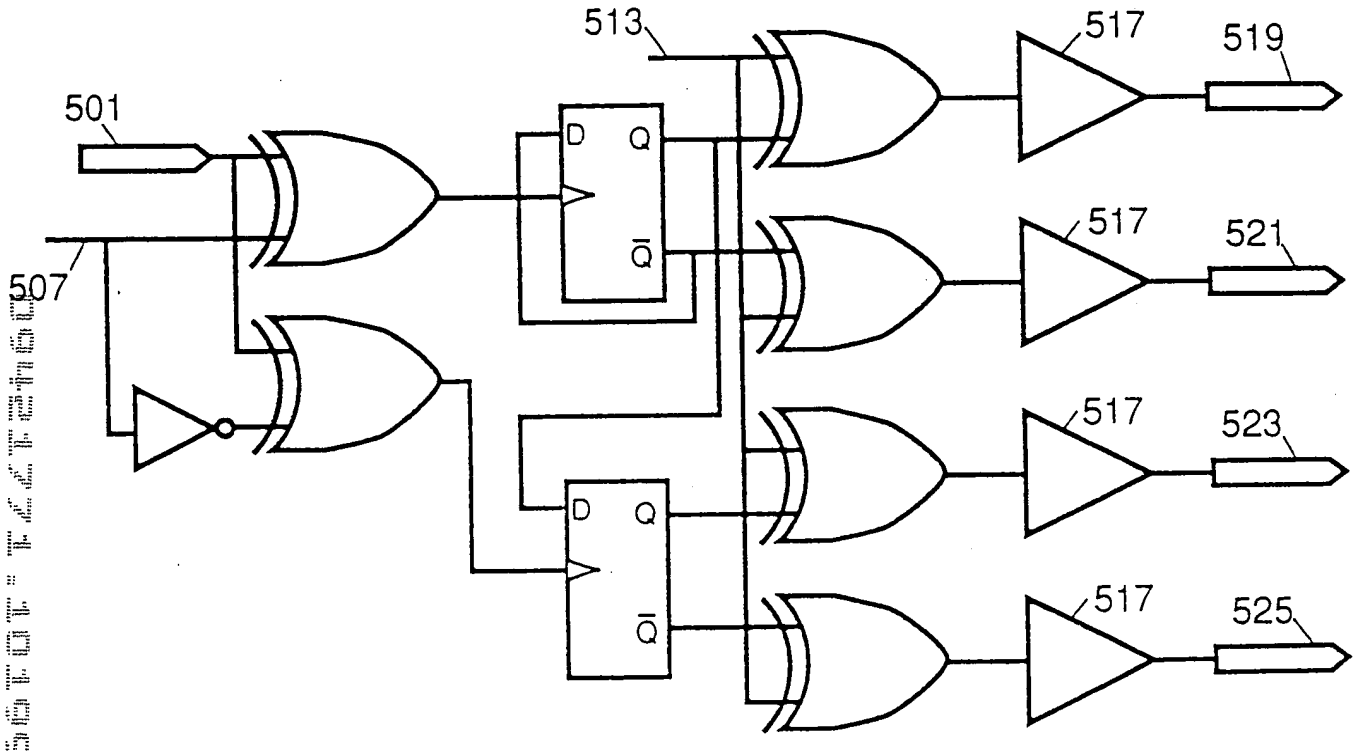


Fig. 5a

500

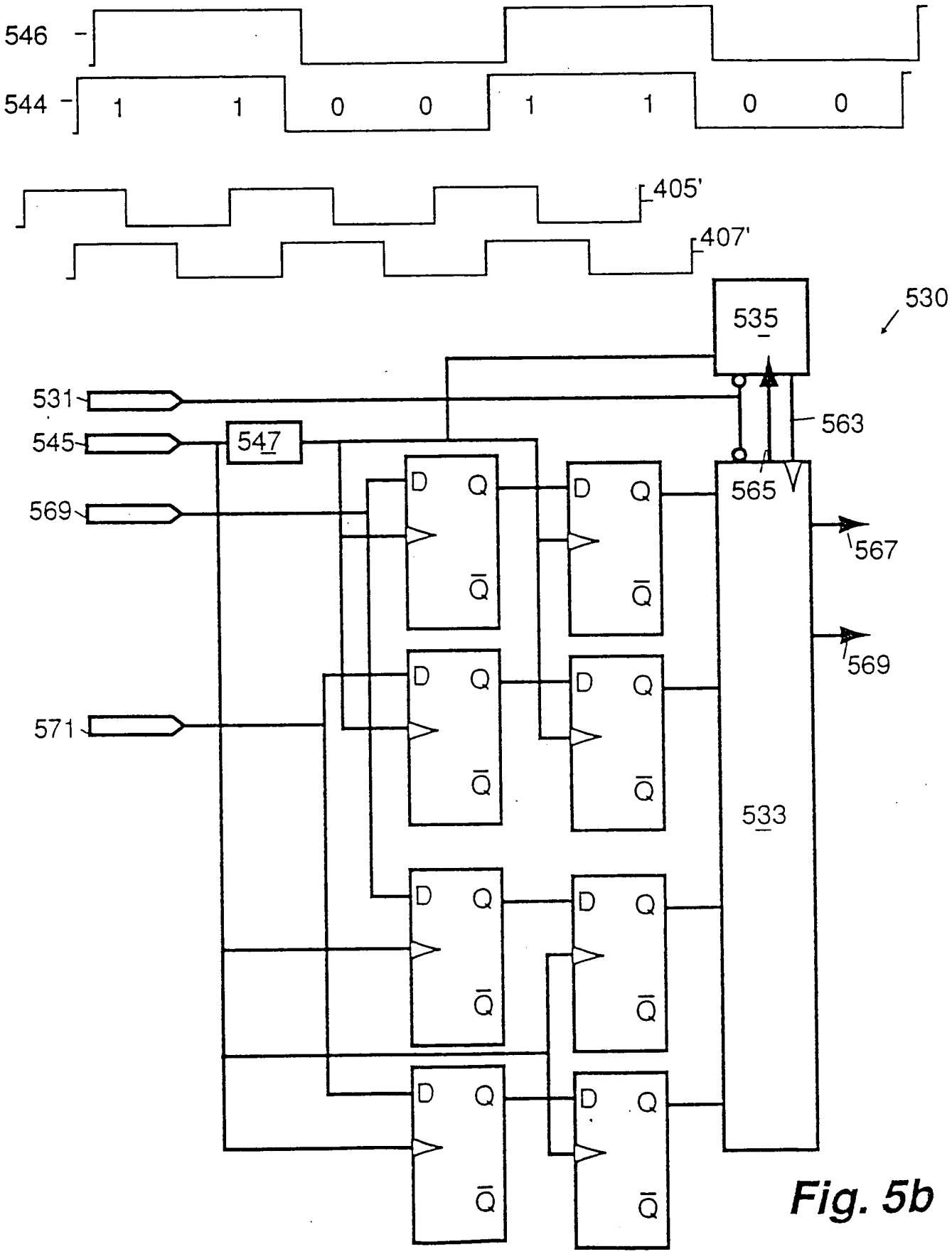

546
544
1
1
0
0
1
1
0
0
405'
407'
530
535
531
545
547
569
571
563
565
567
569
533
D
Q
$\bar{Q}$

Fig. 5b

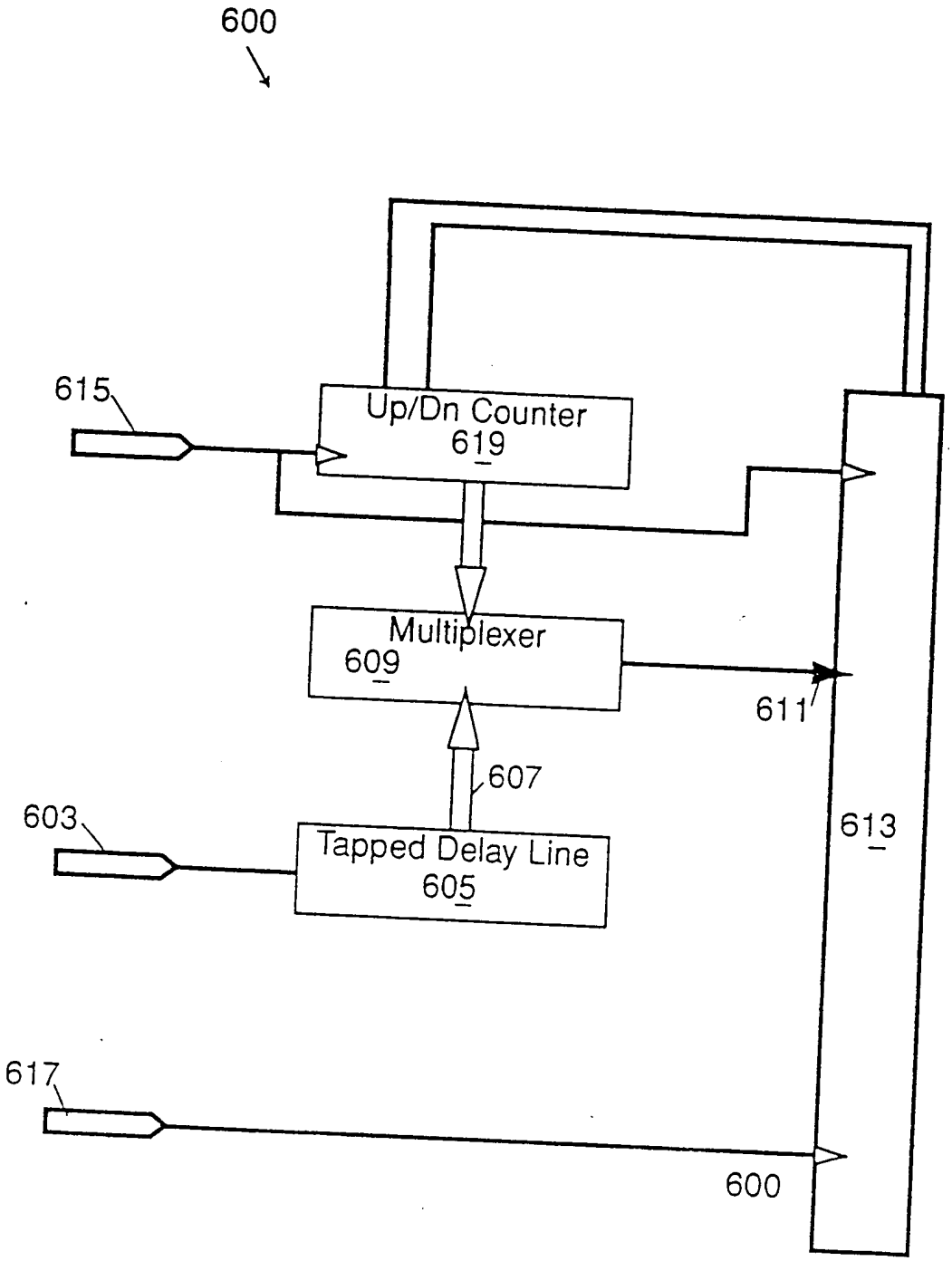

600
615
Up/Dn Counter
619
Multiplexer
609
611
607
603
Tapped Delay Line
605
613
617
600

Fig. 6

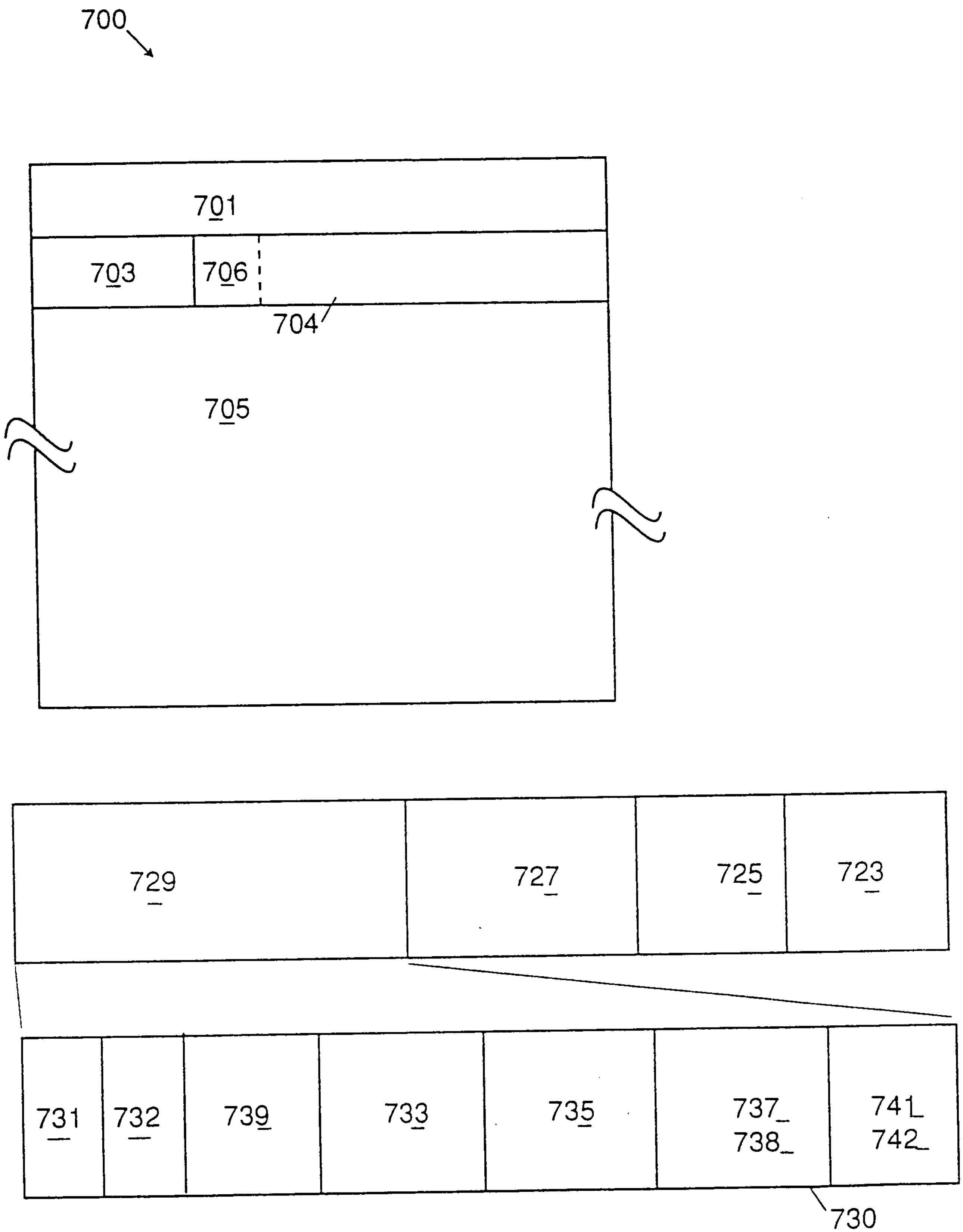

700
701
703
706
704
705
729
727
725
723
731
732
739
733
735
737
738
741
742
730

Fig. 7

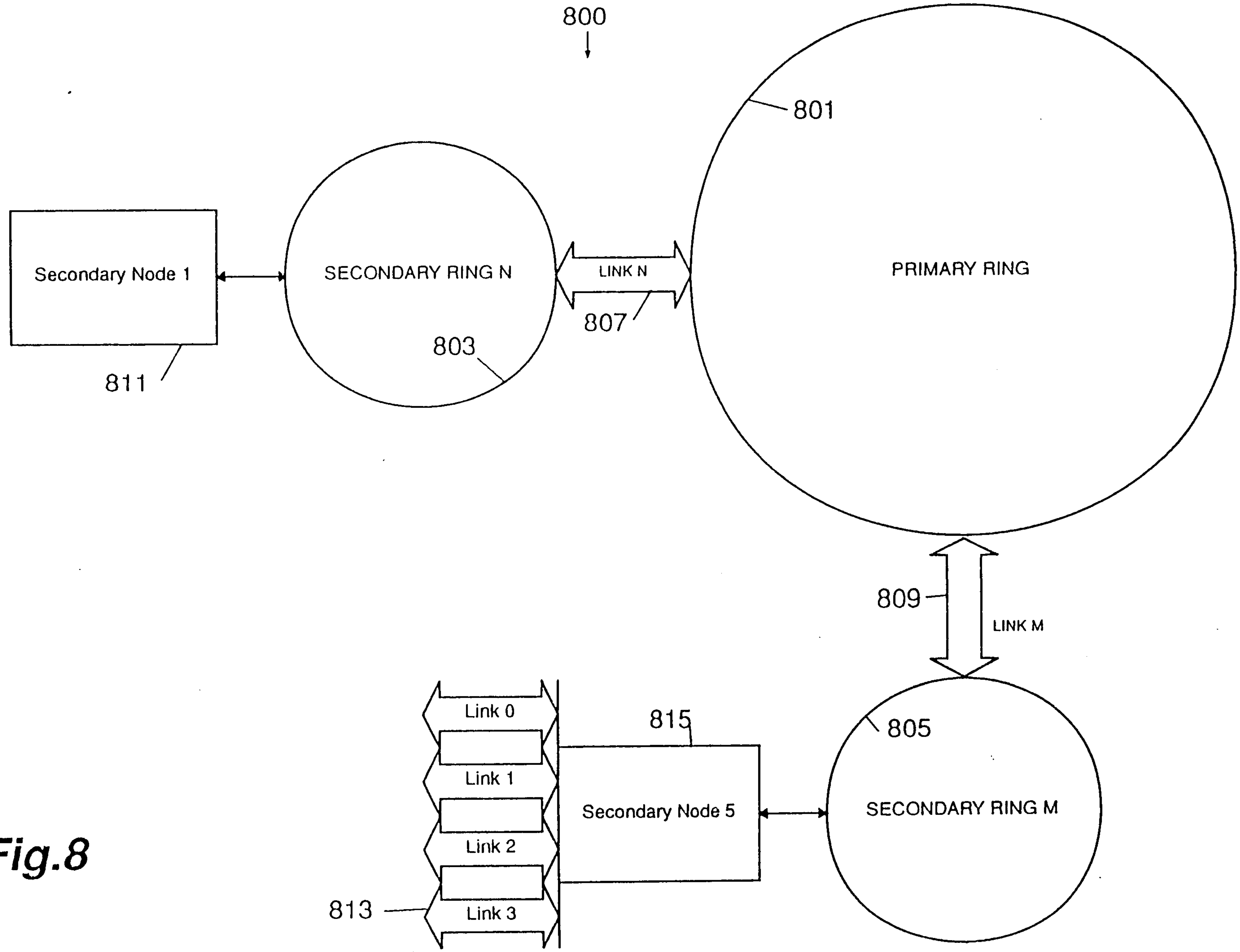

800
801
PRIMARY RING
SECONDARY RING N
803
Secondary Node 1
811
LINK N
807
LINK M
809
SECONDARY RING M
805
Secondary Node 5
815
Link 0
Link 1
Link 2
Link 3
813

Fig.8

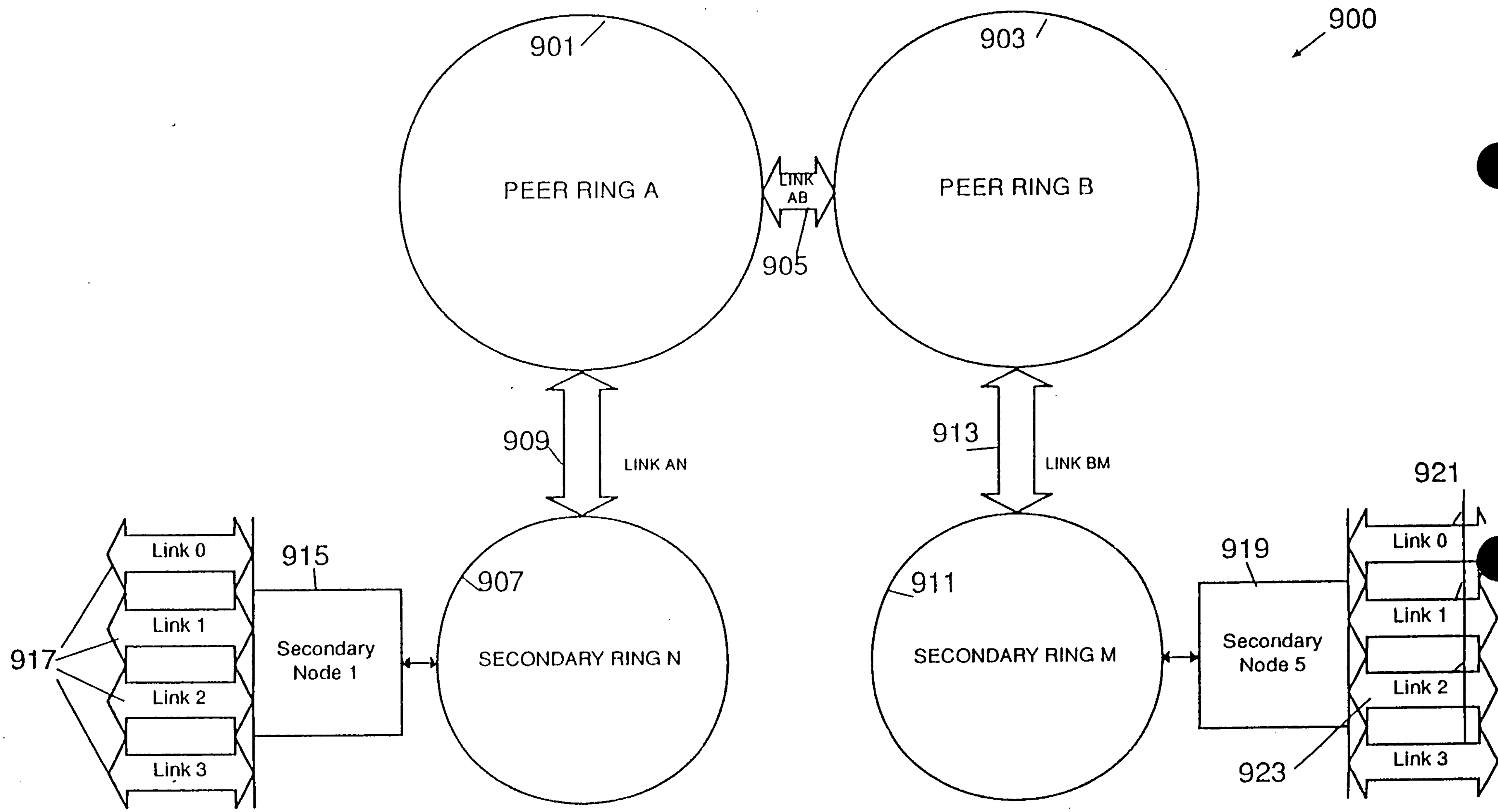

900
901
PEER RING A
LINK AB
905
903
PEER RING B
909
LINK AN
913
LINK BM
907
SECONDARY RING N
911
SECONDARY RING M
915
Secondary Node 1
917
Link 0
Link 1
Link 2
Link 3
919
Secondary Node 5
921
923
Link 0
Link 1
Link 2
Link 3

Fig.9

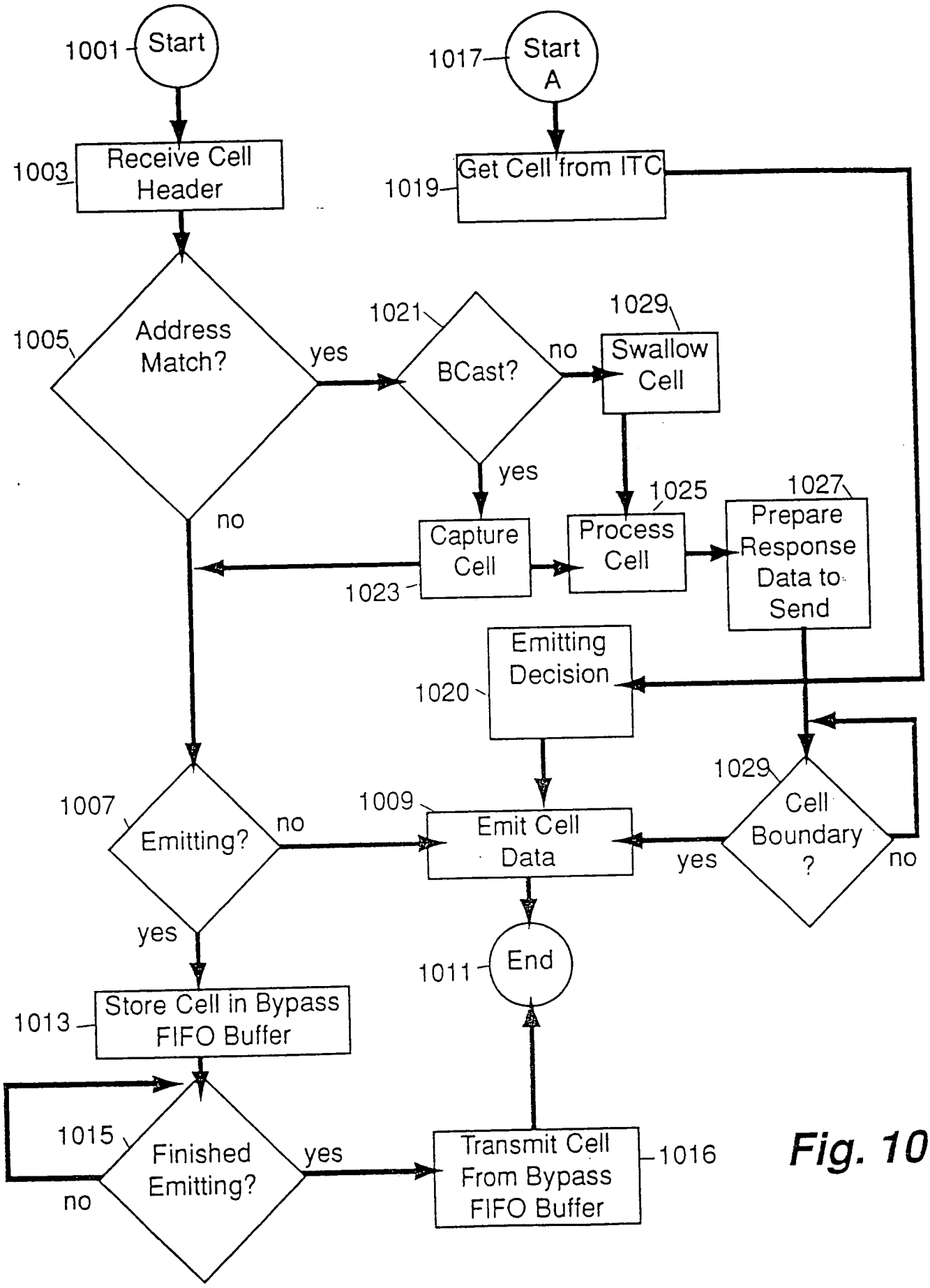


Fig. 10

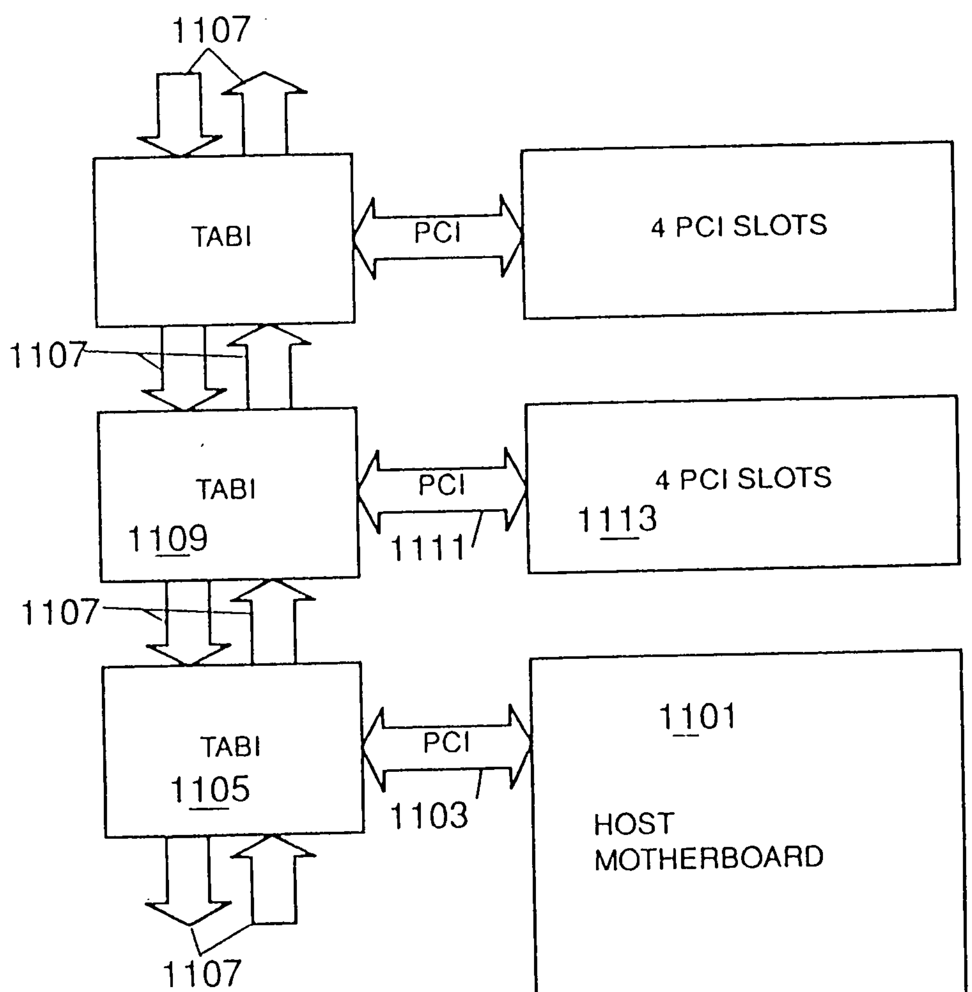
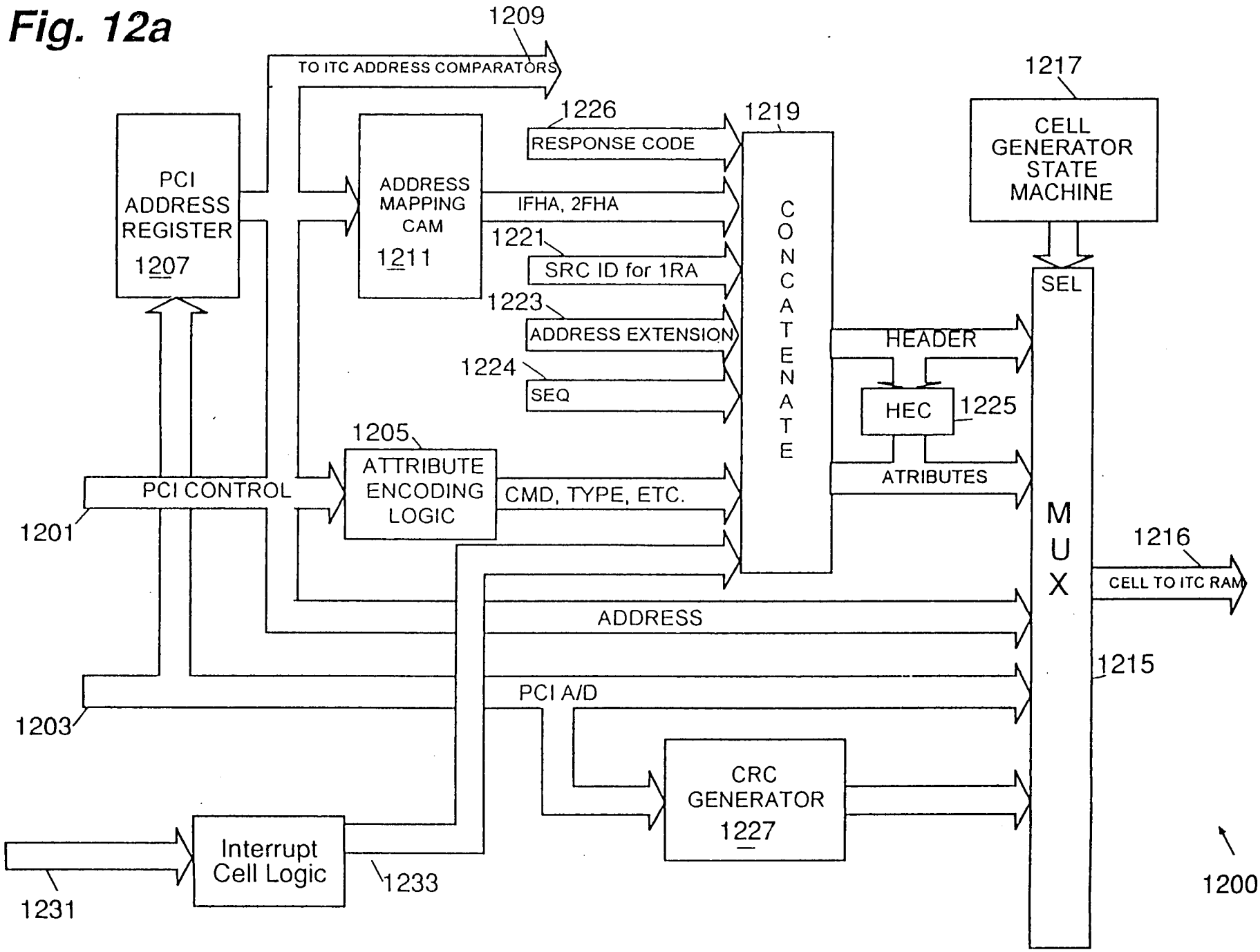


Fig.11

Fig. 12a



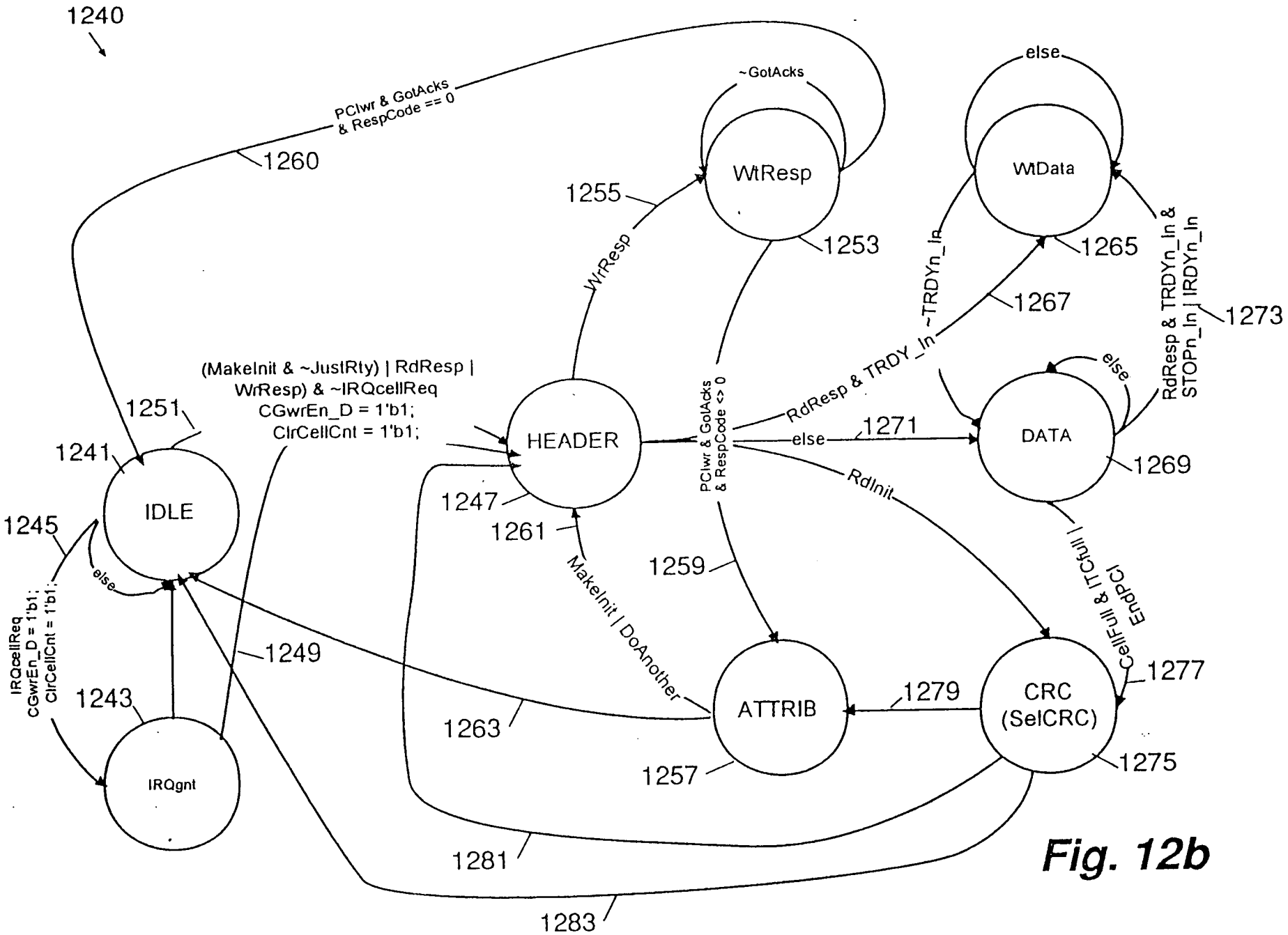

1240
PCIwr & GotAcks
& RespCode == 0
1260
~GotAcks
WtResp
1255
1253
WrResp
else
WtData
1265
1267
~TRDYn_In
RdResp & TRDYn_In &
STOPn_In | IRDYn_In
1273
(MakeInit & ~JustRty) | RdResp |
WrResp) & ~IRQcellReq
CGwrEn_D = 1'b1;
ClrCellCnt = 1'b1;
1251
1241
IDLE
HEADER
PCIwr & GotAcks
& RespCode <> 0
RdResp & TRDY_In
else
1271
DATA
1269
RdInit
1247
1261
MakeInit | DoAnother
1259
1245
else
IRQcellReq
CGwrEn_D = 1'b1;
ClrCellCnt = 1'b1;
1249
1243
IRQgnt
1263
ATTRIB
1257
1279
CRC
(SelCRC)
1275
CellFull & TCfull |
EndPCI
1277
1281
1283

Fig. 12b

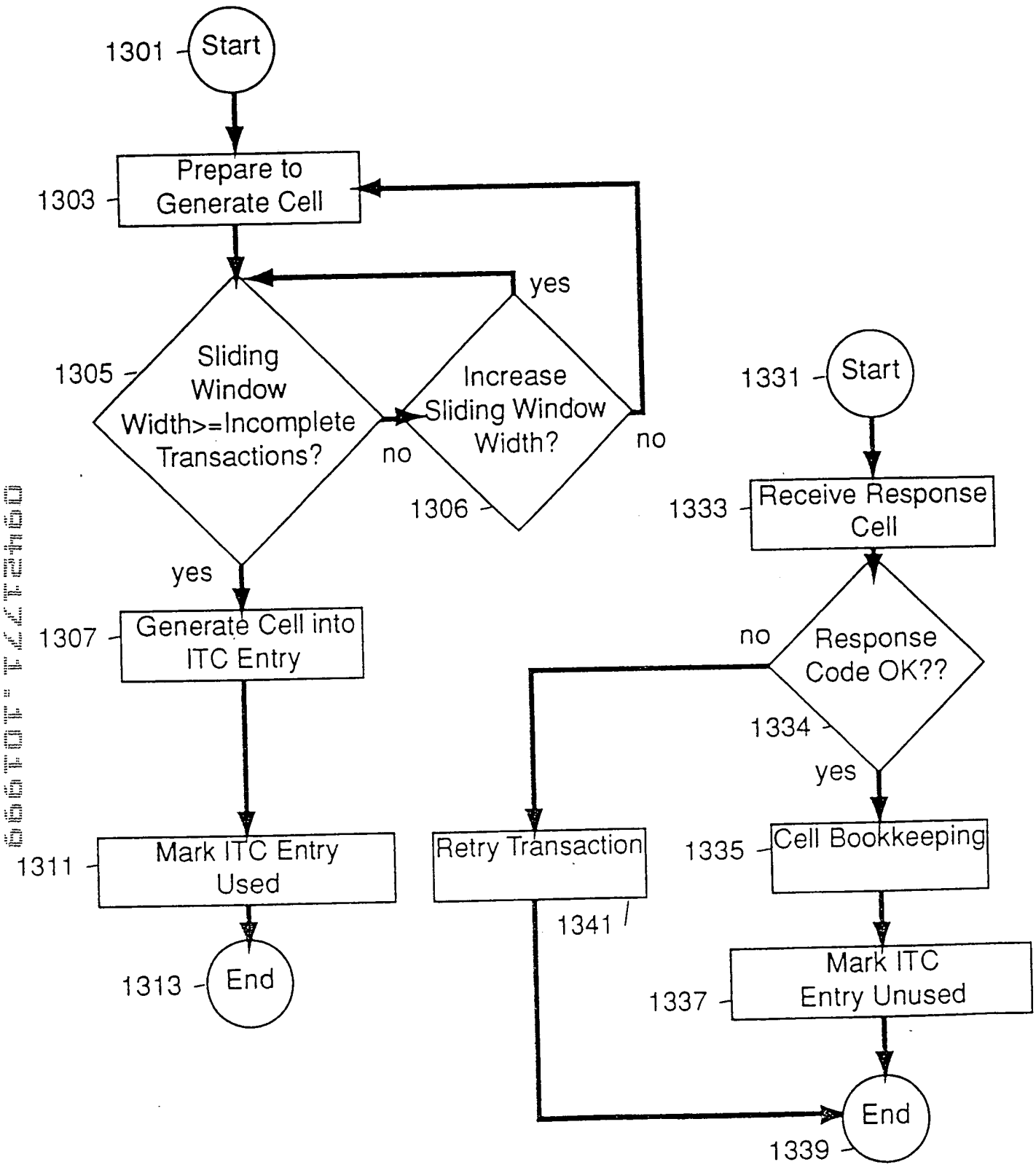

1301
Start
Prepare to Generate Cell
1303
Sliding Window Width>=Incomplete Transactions?
1305
yes
no
Increase Sliding Window Width?
1306
yes
no
Generate Cell into ITC Entry
1307
Mark ITC Entry Used
1311
End
1313
1331
Start
Receive Response Cell
1333
Response Code OK??
1334
no
yes
Retry Transaction
1341
Cell Bookkeeping
1335
Mark ITC Entry Unused
1337
End
1339

Fig. 13a

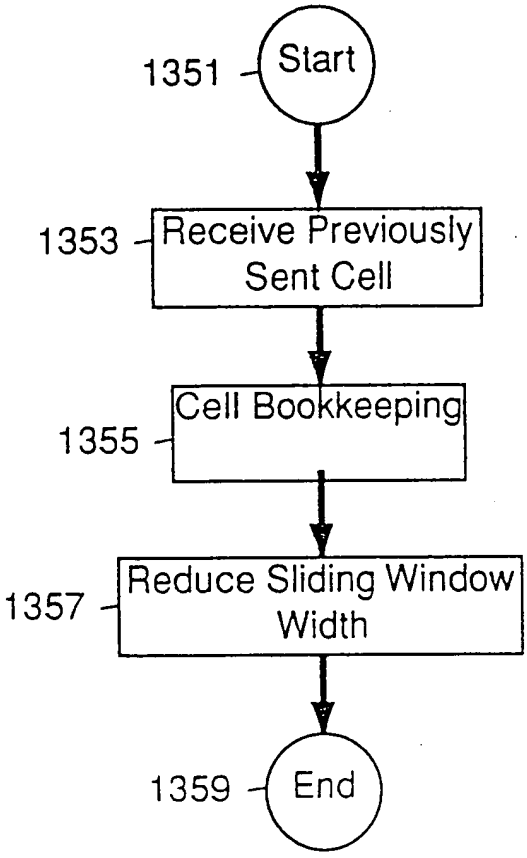
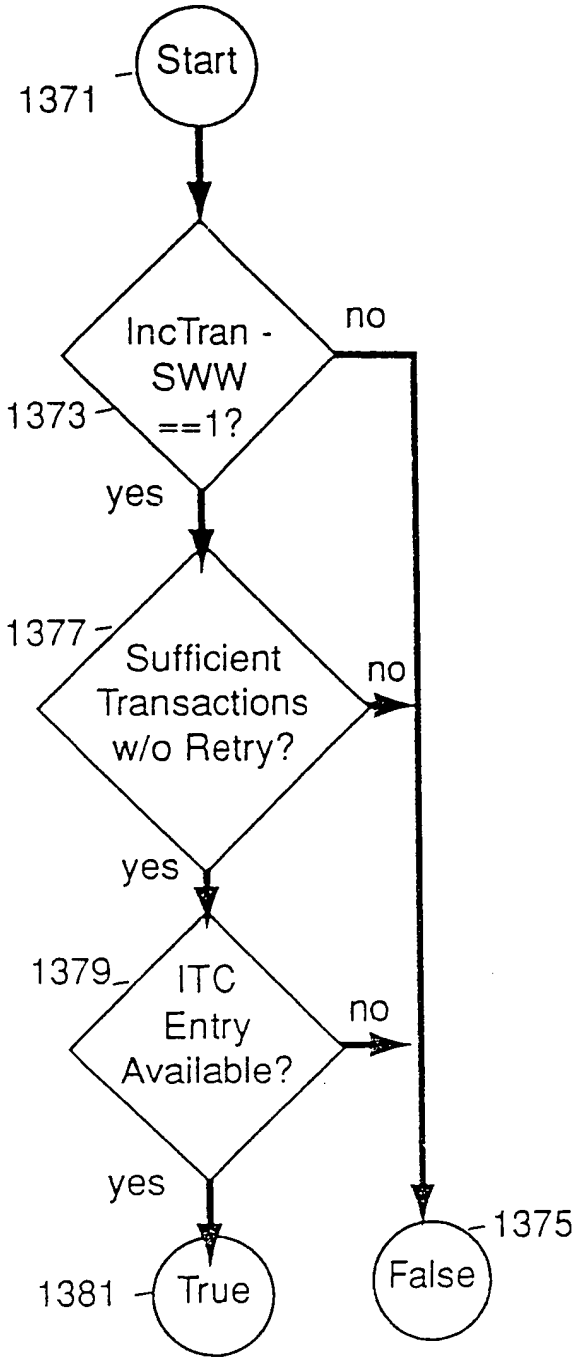

1351
Start
1353
Receive Previously Sent Cell
1355
Cell Bookkeeping
1357
Reduce Sliding Window Width
1359
End

Fig. 13b


1371
Start
1373
IncTran - SWW ==1?
no
yes
1377
Sufficient Transactions w/o Retry?
no
yes
1379
ITC Entry Available?
no
yes
1375
1381
True
False

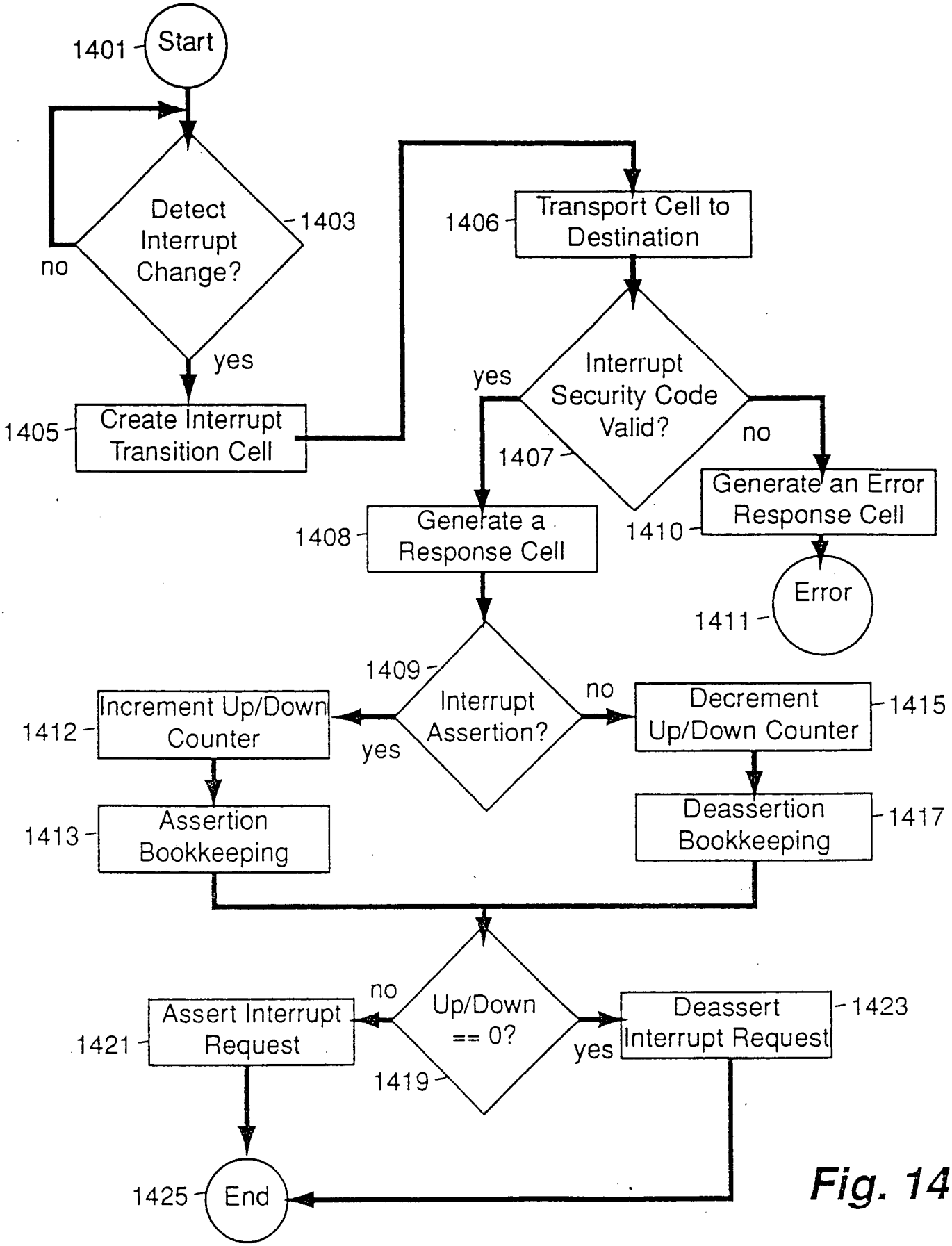
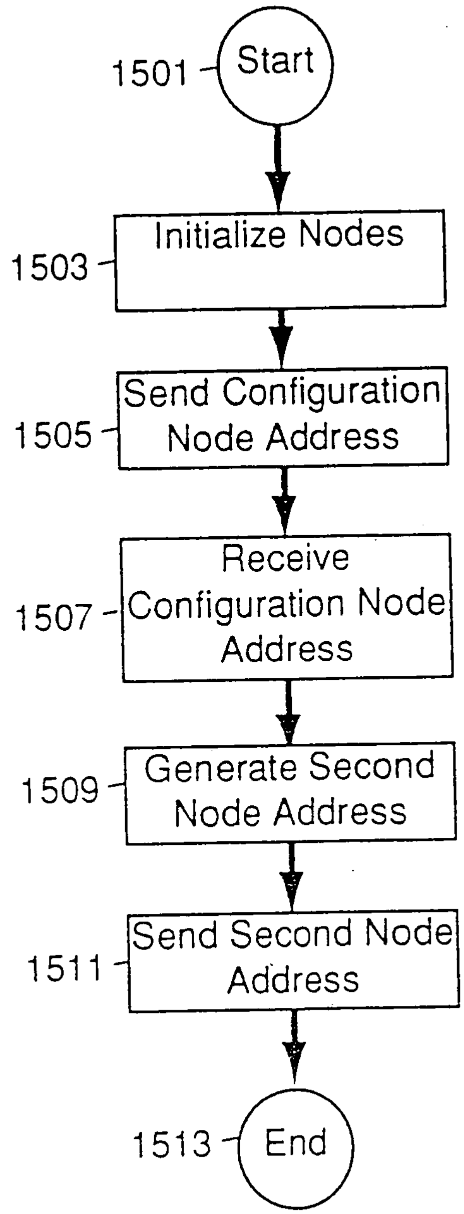

1401
Start
Detect Interrupt Change?
1403
no
yes
1405
Create Interrupt Transition Cell
1406
Transport Cell to Destination
Interrupt Security Code Valid?
1407
yes
no
1408
Generate a Response Cell
1410
Generate an Error Response Cell
1411
Error
1409
Interrupt Assertion?
yes
no
1412
Increment Up/Down Counter
1415
Decrement Up/Down Counter
1413
Assertion Bookkeeping
1417
Deassertion Bookkeeping
Up/Down == 0?
1419
no
yes
1421
Assert Interrupt Request
1423
Deassert Interrupt Request
1425
End

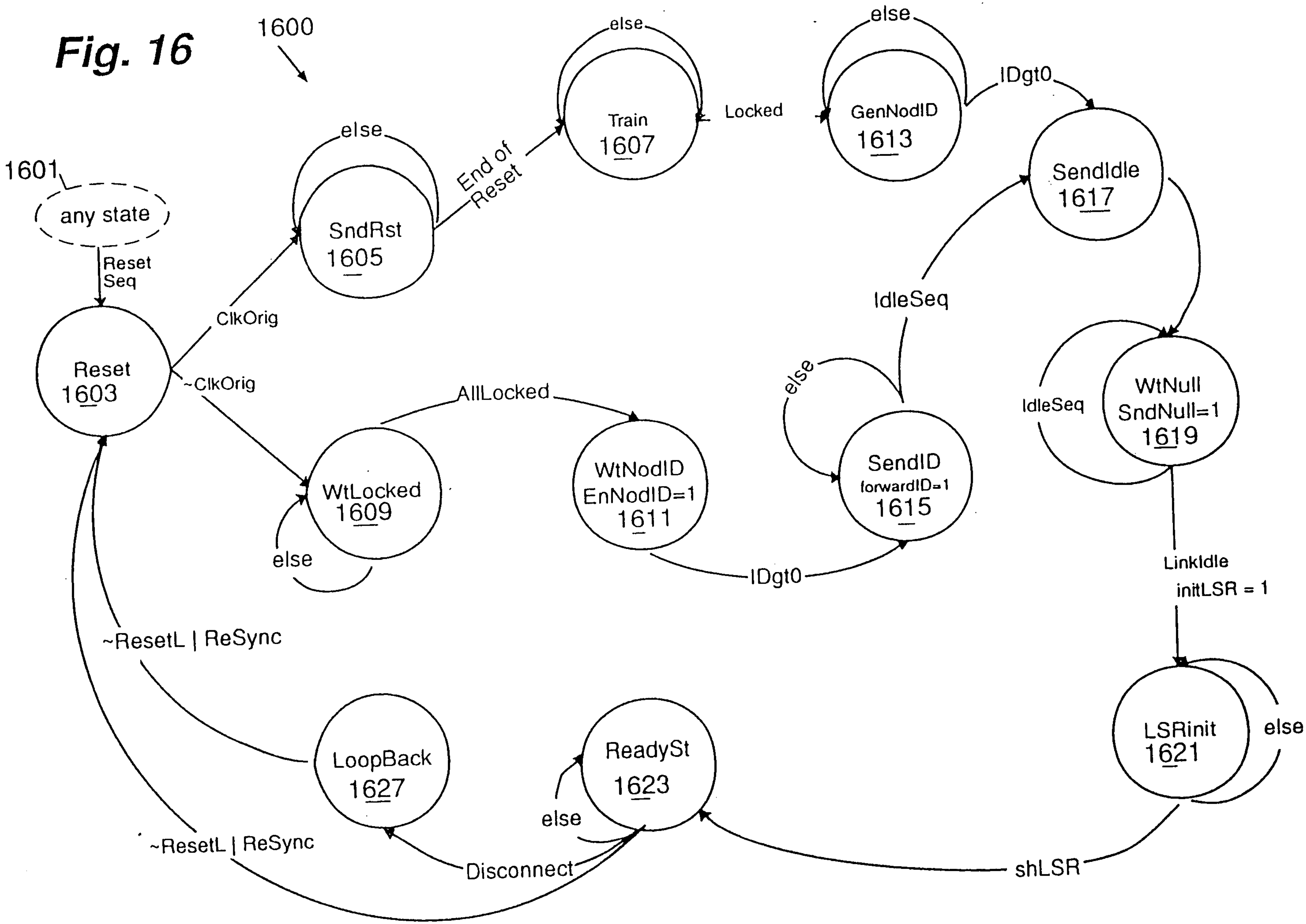
Fig. 14



1501
Start
1503
Initialize Nodes
1505
Send Configuration Node Address
1507
Receive Configuration Node Address
1509
Generate Second Node Address
1511
Send Second Node Address
1513
End

Fig. 15

Fig. 16



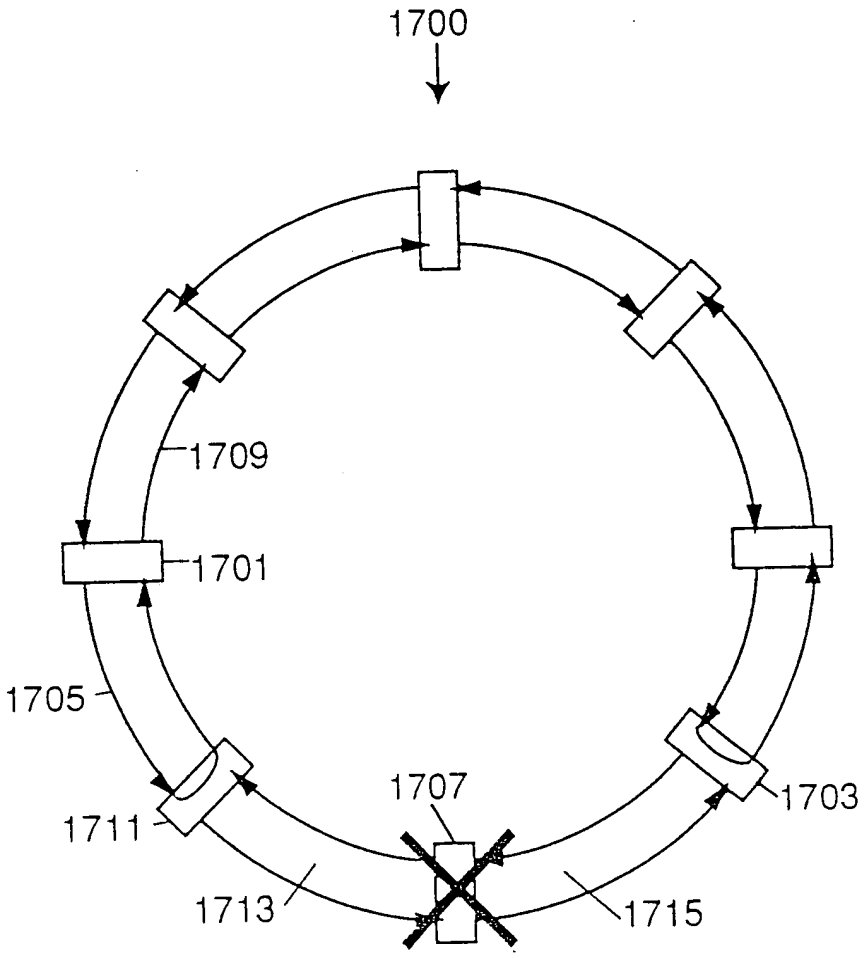


Fig. 17

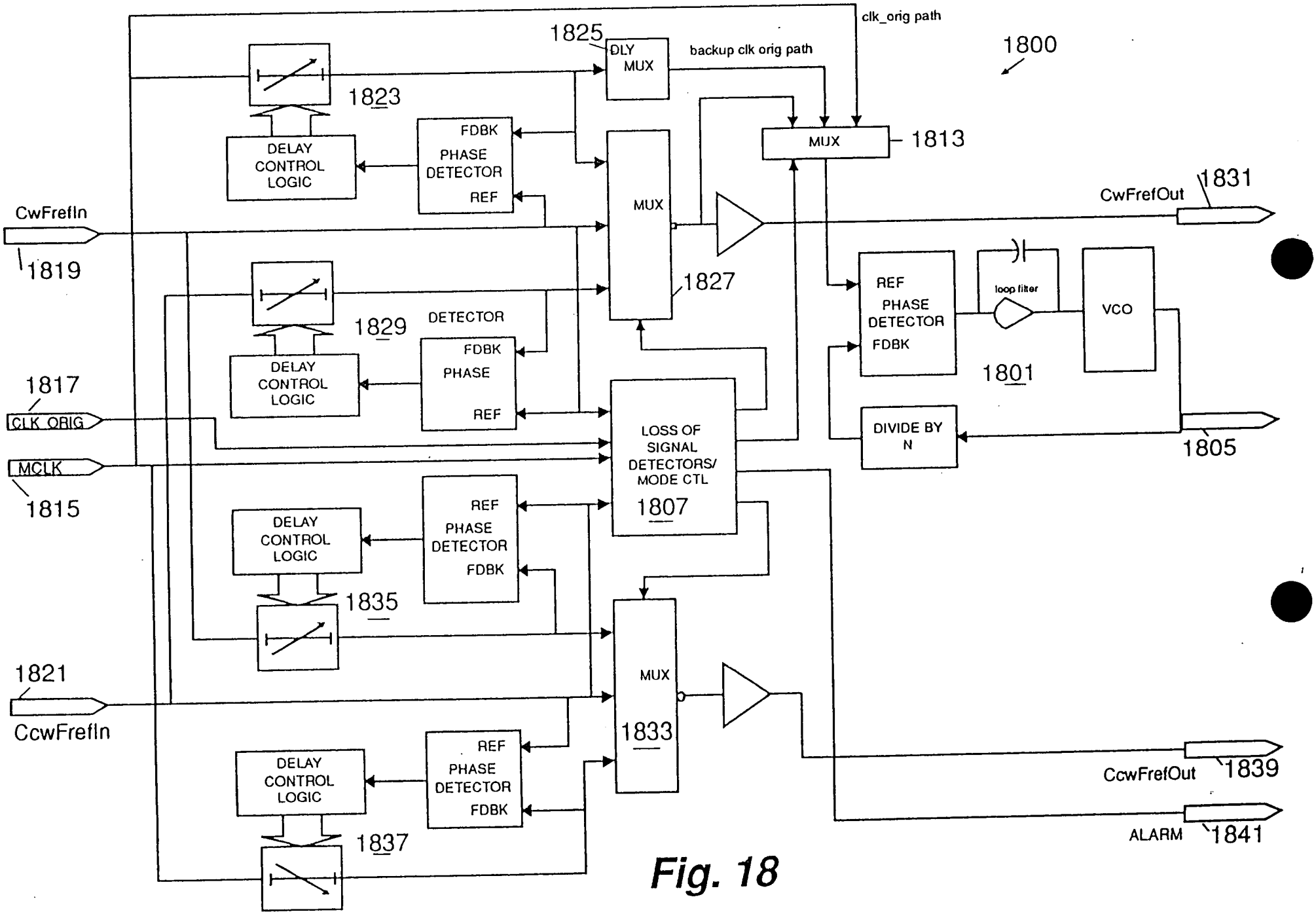

clk_orig path
1825
DLY MUX
backup clk orig path
1800
1823
DELAY CONTROL LOGIC
FDBK
PHASE DETECTOR
REF
MUX
1813
MUX
1827
1831
CwFrefOut
CwFrefIn
1819
1829
DETECTOR
DELAY CONTROL LOGIC
FDBK
PHASE
REF
REF
PHASE DETECTOR
FDBK
loop filter
VCO
1801
1817
CLK_ORIG
MCLK
1815
LOSS OF SIGNAL DETECTORS/ MODE CTL
1807
DIVIDE BY N
1805
DELAY CONTROL LOGIC
REF
PHASE DETECTOR
FDBK
1835
1821
CcwFrefIn
MUX
1833
DELAY CONTROL LOGIC
REF
PHASE DETECTOR
FDBK
CcwFrefOut
1839
1837
ALARM
1841

Fig. 18

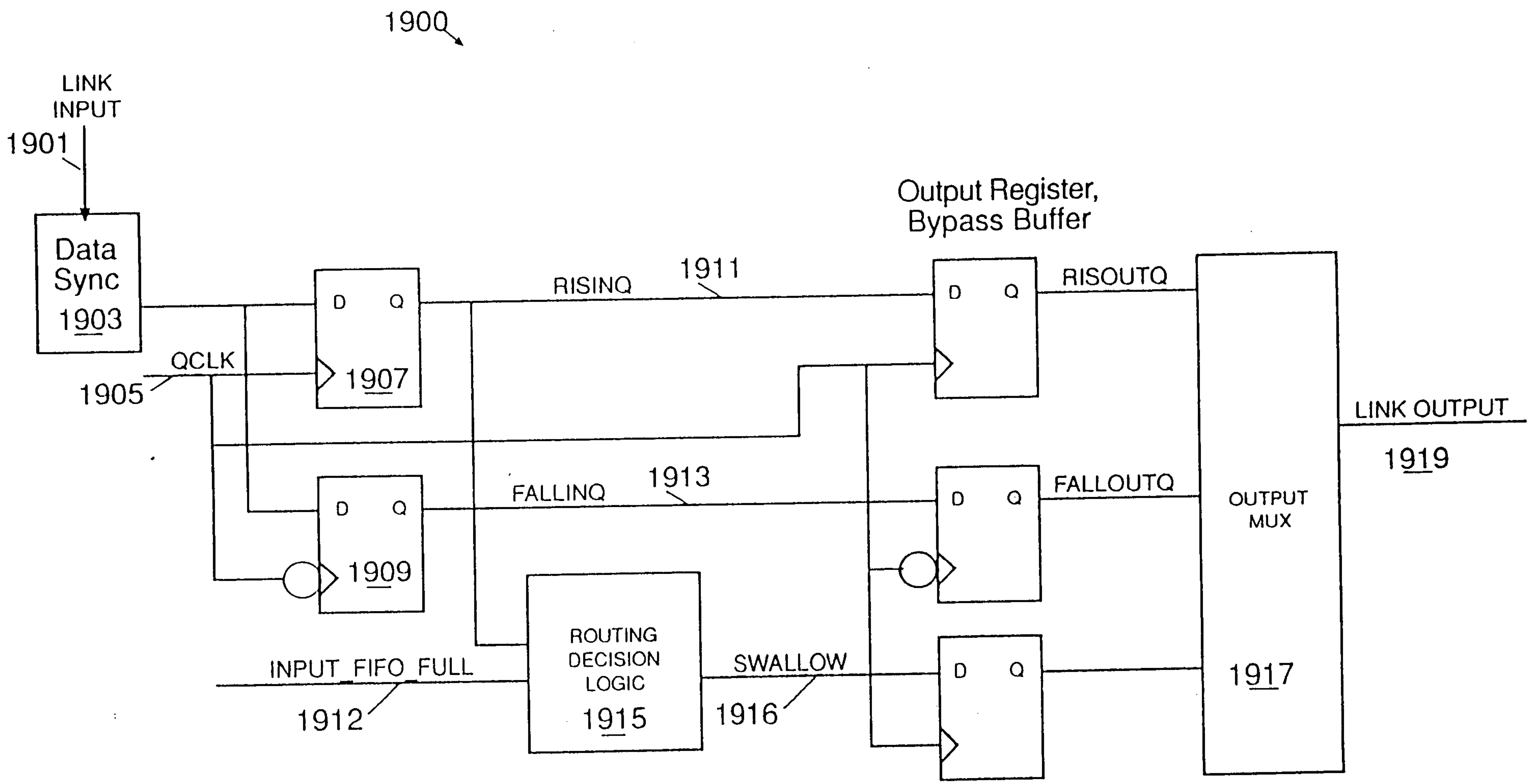

1900
LINK INPUT
1901
Data Sync 1903
QCLK
1905
D
Q
1907
D
Q
1909
RISINQ
1911
FALLINQ
1913
INPUT_FIFO_FULL
1912
ROUTING DECISION LOGIC
1915
SWALLOW
1916
Output Register, Bypass Buffer
D
Q
RISOUTQ
D
Q
FALLOUTQ
D
Q
OUTPUT MUX
1917
LINK OUTPUT
1919

Fig. 19a

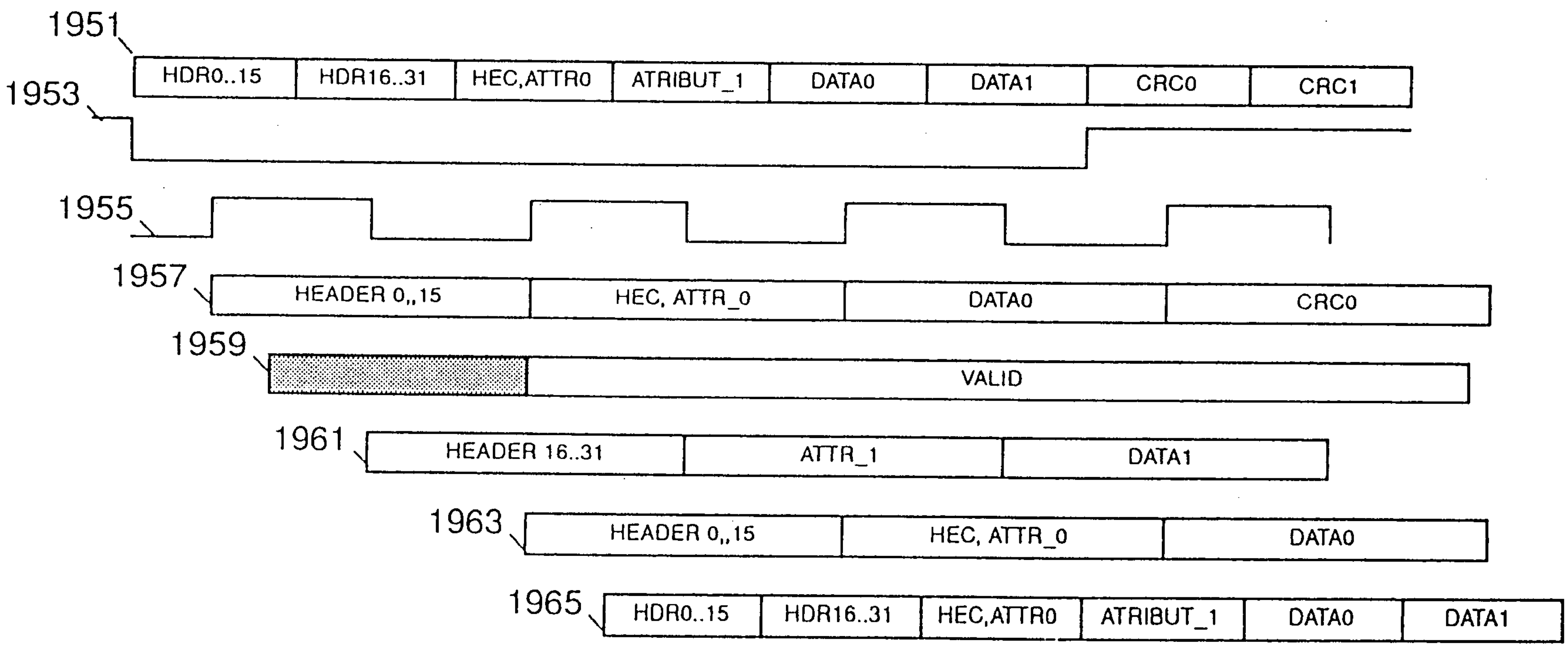

1951
HDR0..15
HDR16..31
HEC,ATTR0
ATRIBUT_1
DATA0
DATA1
CRC0
CRC1
1953
1955
1957
HEADER 0,,15
HEC, ATTR_0
DATA0
CRC0
1959
VALID
1961
HEADER 16..31
ATTR_1
DATA1
1963
HEADER 0,,15
HEC, ATTR_0
DATA0
1965
HDR0..15
HDR16..31
HEC,ATTR0
ATRIBUT_1
DATA0
DATA1

Fig. 19b

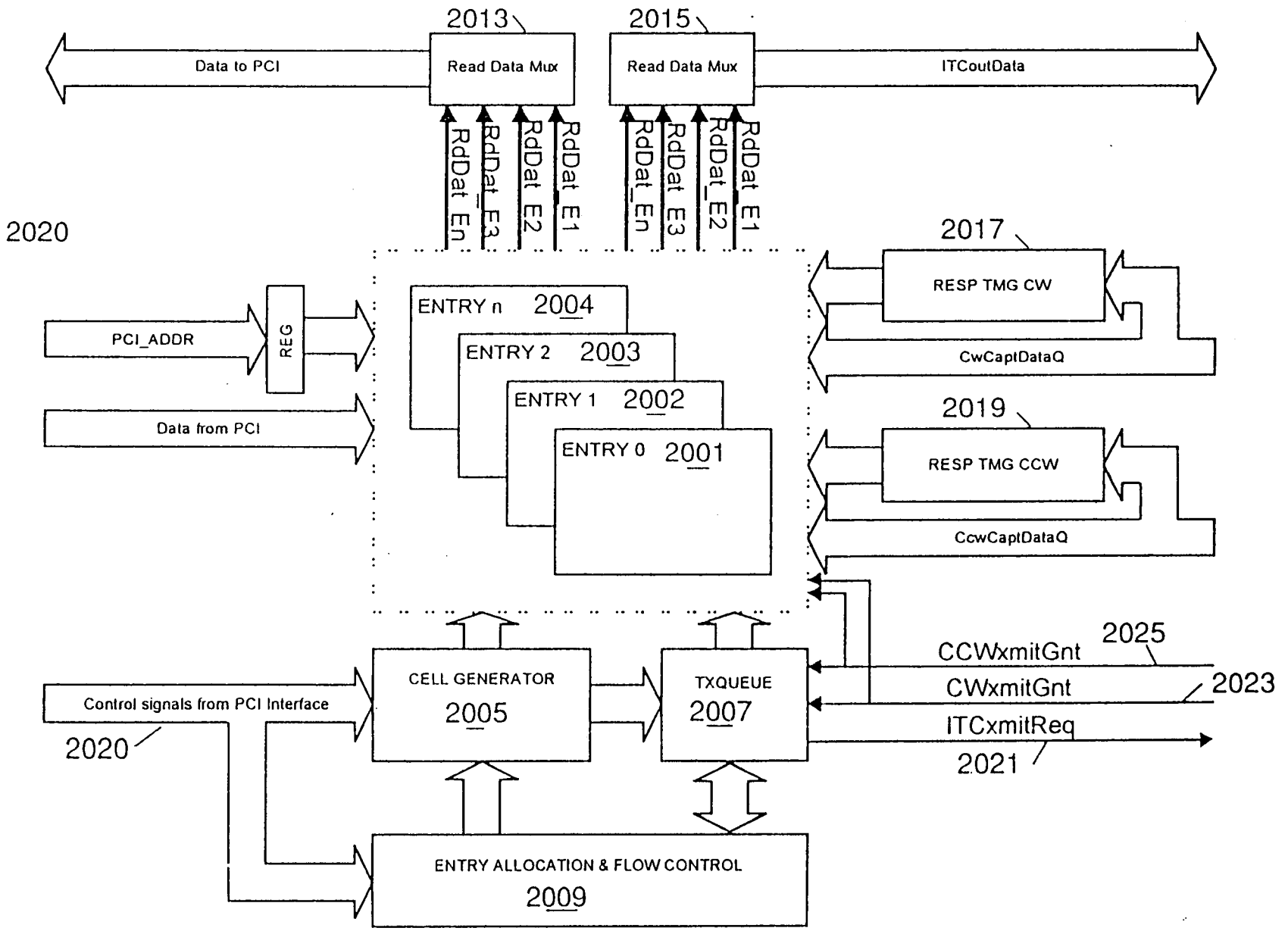

2013
2015
Data to PCI
Read Data Mux
Read Data Mux
ITCoutData
RdDat_En
RdDat_E3
RdDat_E2
RdDat_E1
RdDat_En
RdDat_E3
RdDat_E2
RdDat_E1
2020
2017
RESP TMG CW
CwCaptDataQ
PCI_ADDR
REG
ENTRY n 2004
ENTRY 2 2003
ENTRY 1 2002
ENTRY 0 2001
Data from PCI
2019
RESP TMG CCW
CcwCaptDataQ
2025
CCWxmitGnt
CWxmitGnt
2023
ITCxmitReq
2021
CELL GENERATOR
2005
TXQUEUE
2007
Control signals from PCI Interface
2020
ENTRY ALLOCATION & FLOW CONTROL
2009
2000

Fig. 20

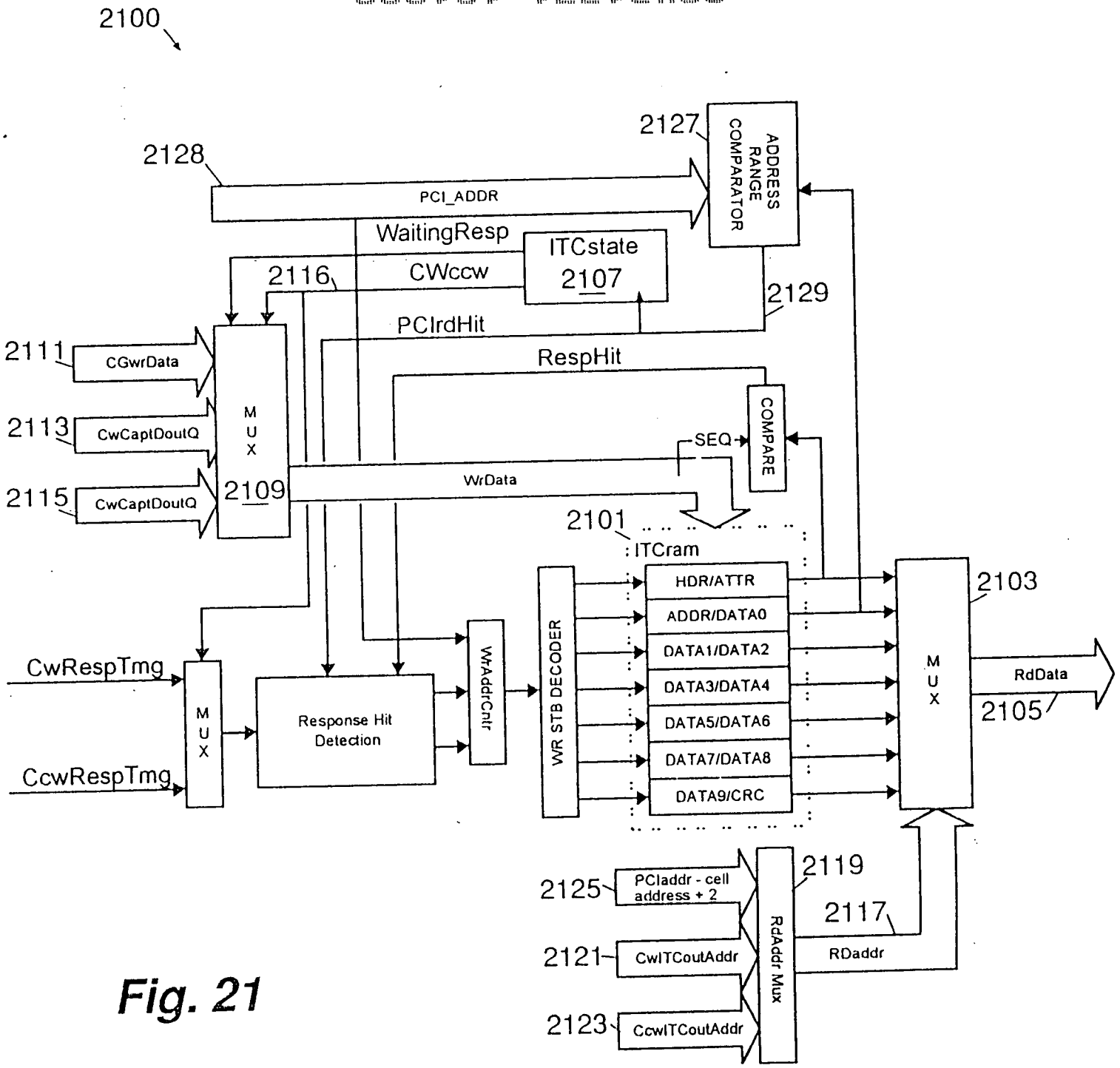


Fig. 21

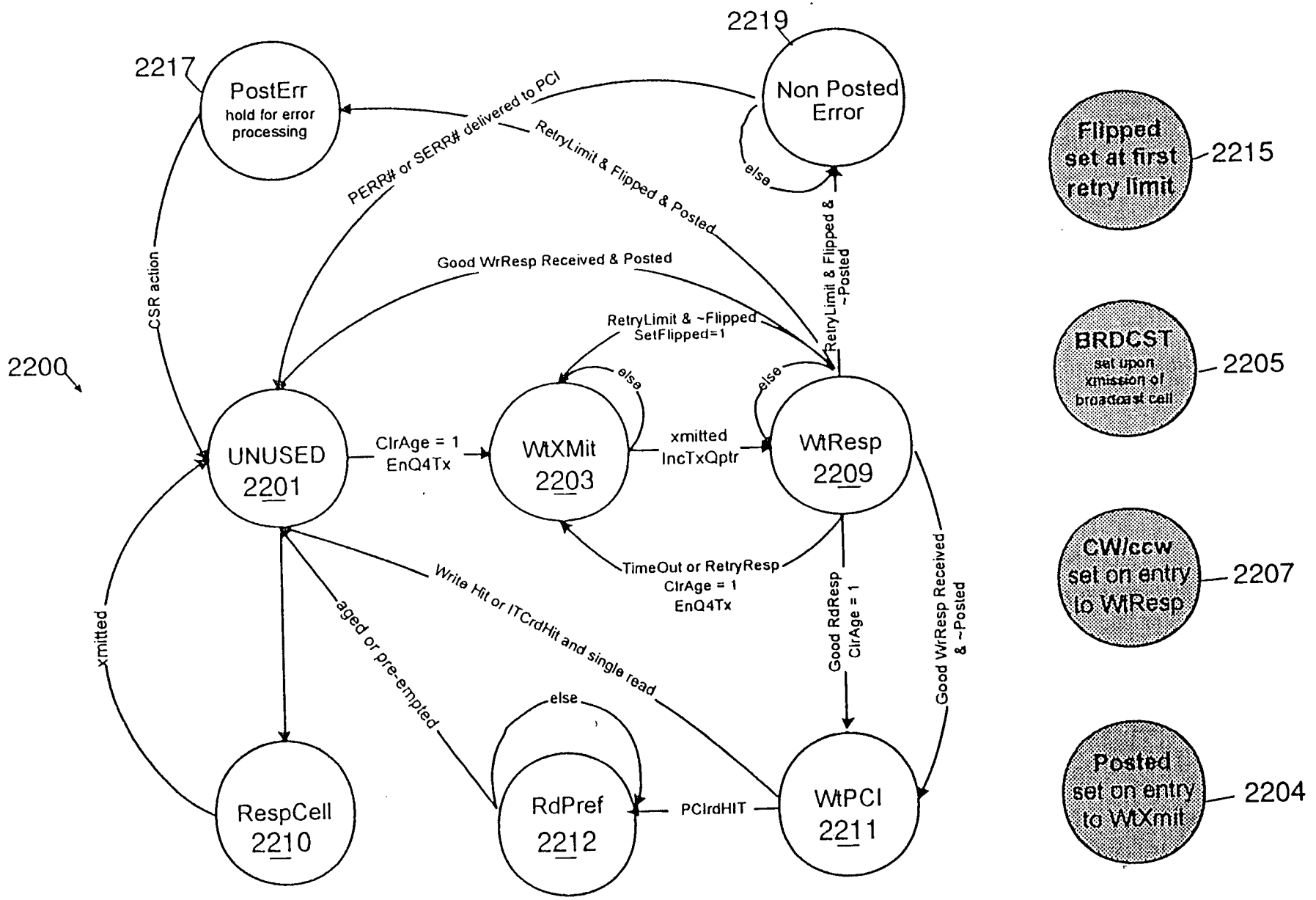

2200
2217
PostErr
hold for error processing
2219
Non Posted Error
PERR# or SERR# delivered to PCI
RetryLimit & Flipped & Posted
else
CSR action
Good WrResp Received & Posted
RetryLimit & Flipped & ~Posted
RetryLimit & ~Flipped
SetFlipped=1
else
else
UNUSED
2201
ClrAge = 1
EnQ4Tx
WtXMit
2203
xmitted
IncTxQptr
WtResp
2209
TimeOut or RetryResp
ClrAge = 1
EnQ4Tx
Write Hit or ITCrdHit and single read
aged or pre-empted
xmitted
Good RdResp
ClrAge = 1
Good WrResp Received
& ~Posted
else
RespCell
2210
RdPref
2212
PCIrdHIT
WtPCI
2211
Flipped
set at first
retry limit
2215
BRDCST
set upon
xmission of
broadcast cell
2205
CW/ccw
set on entry
to WtResp
2207
Posted
set on entry
to WtXmit
2204

Fig. 22